FIG. 1

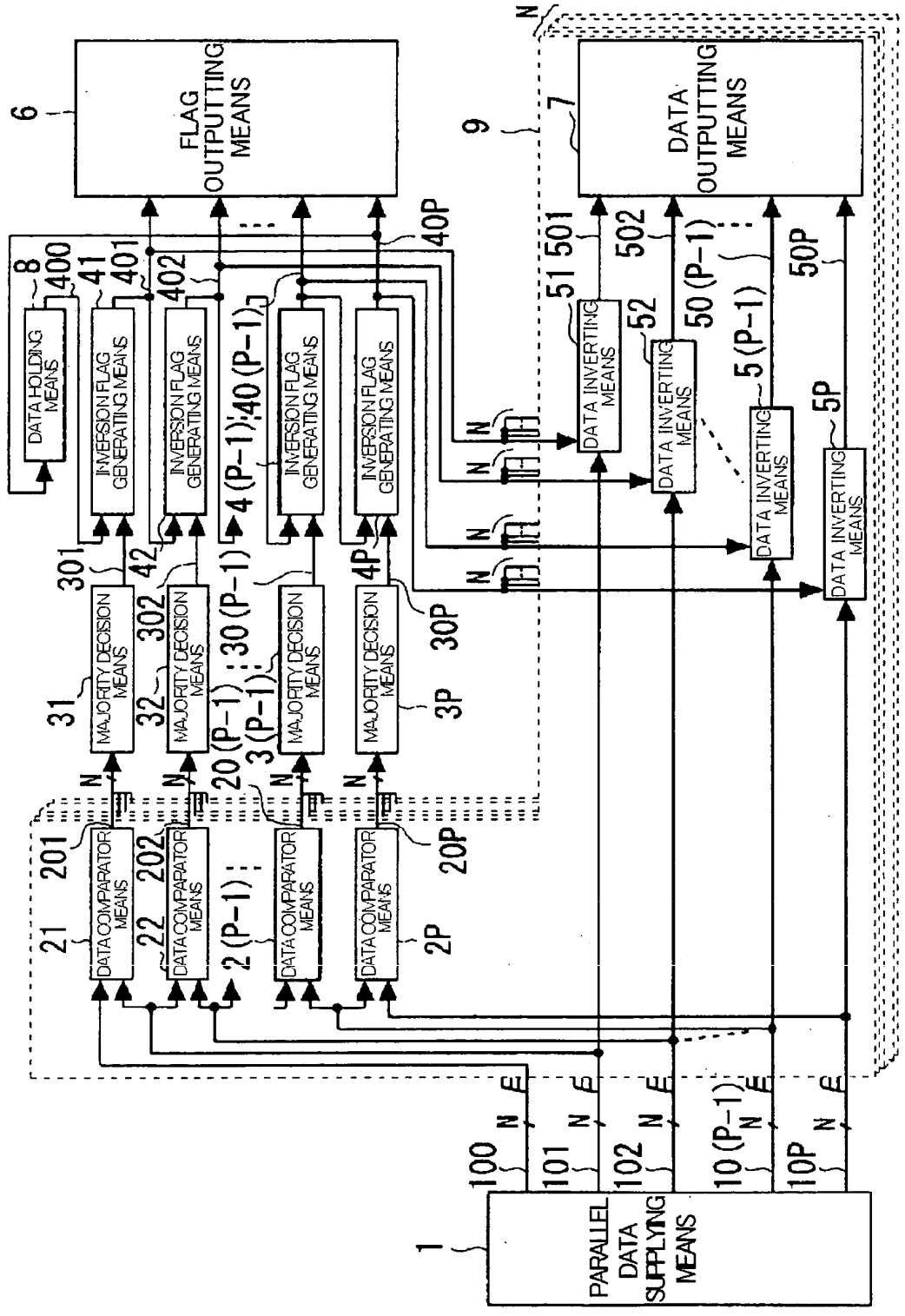

PARALLEL DATA SUPPLYING MEANS
1
100
101
102
10 (P-1)
10P
N
DATA COMPARATOR MEANS
21
201
22
202
2 (P-1)
2P
20P
MAJORITY DECISION MEANS
31
301
32
302
3 (P-1)
3P
30P
INVERSION FLAG GENERATING MEANS
41
401
42
402
4 (P-1)
4P
40P
DATA HOLDING MEANS
8
400
FLAG OUTPUTTING MEANS
6
9
DATA INVERTING MEANS
51
501
52
502
5 (P-1)
5P
50 (P-1)
50P
DATA OUTPUTTING MEANS
7

FIG. 2

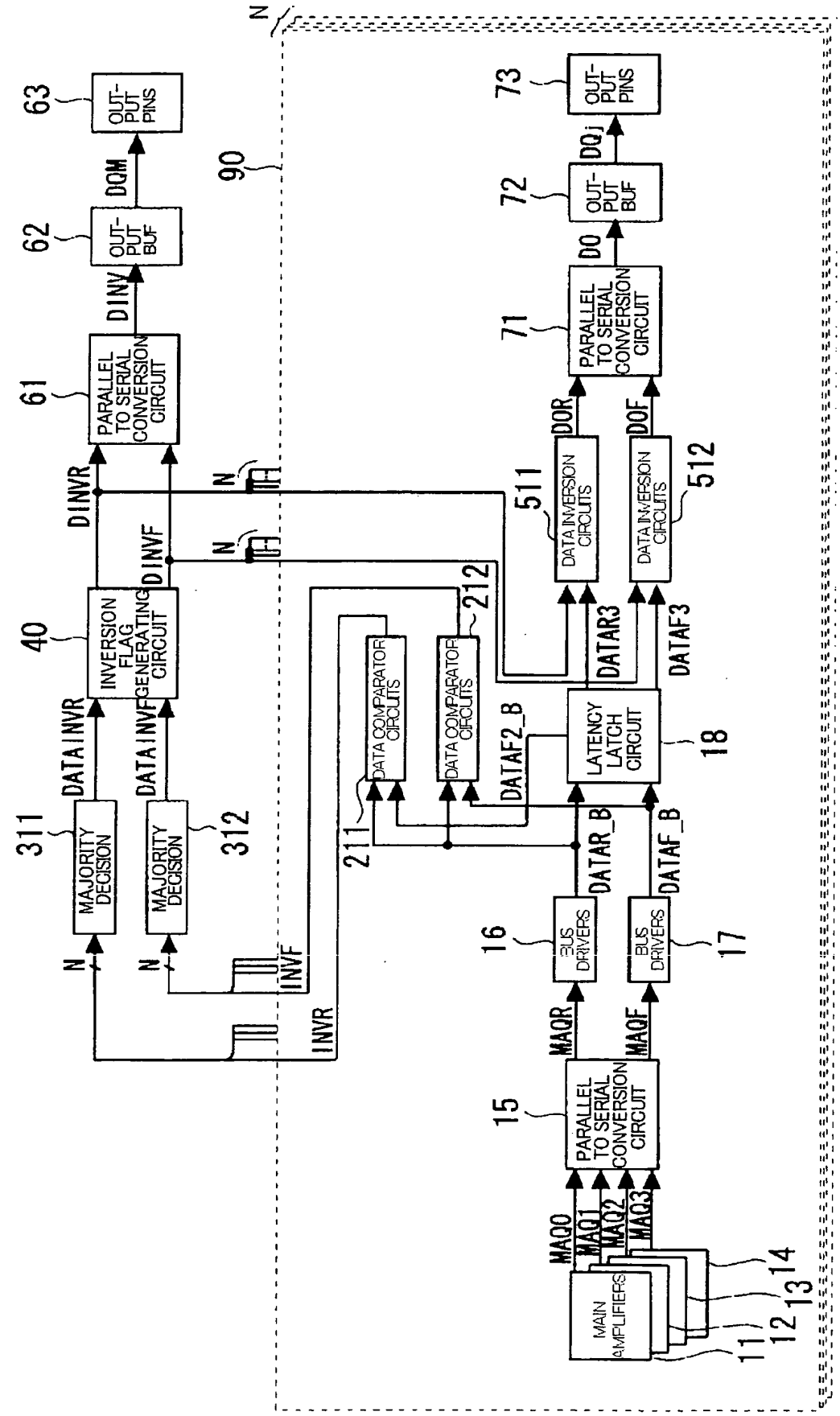

MAIN AMPLIFIERS
11
12
13
14
MAQ0
MAQ1
MAQ2
MAQ3
PARALLEL TO SERIAL CONVERSION CIRCUIT
15
MAQR
MAQF
BUS DRIVERS
16
BUS DRIVERS
17
DATAR_B
DATAF_B
LATENCY LATCH CIRCUIT
18
DATAF2_B
DATA COMPARATOR CIRCUITS
211
DATA COMPARATOR CIRCUITS
212
DATAR3
DATAF3
DATA INVERSION CIRCUITS
511
DATA INVERSION CIRCUITS
512
DOR
DOF
PARALLEL TO SERIAL CONVERSION CIRCUIT
71
DO
OUT-PUT BUF
72
DQj
OUT-PUT PINS
73
INVR
INVF
N
MAJORITY DECISION
311
MAJORITY DECISION
312
DATAINVR
DATAINVF
INVERSION FLAG GENERATING CIRCUIT
40
DINVR
DINVF
PARALLEL TO SERIAL CONVERSION CIRCUIT
61
DINV
OUT-PUT BUF
62
DQM
OUT-PUT PINS
63
90

FIG. 3

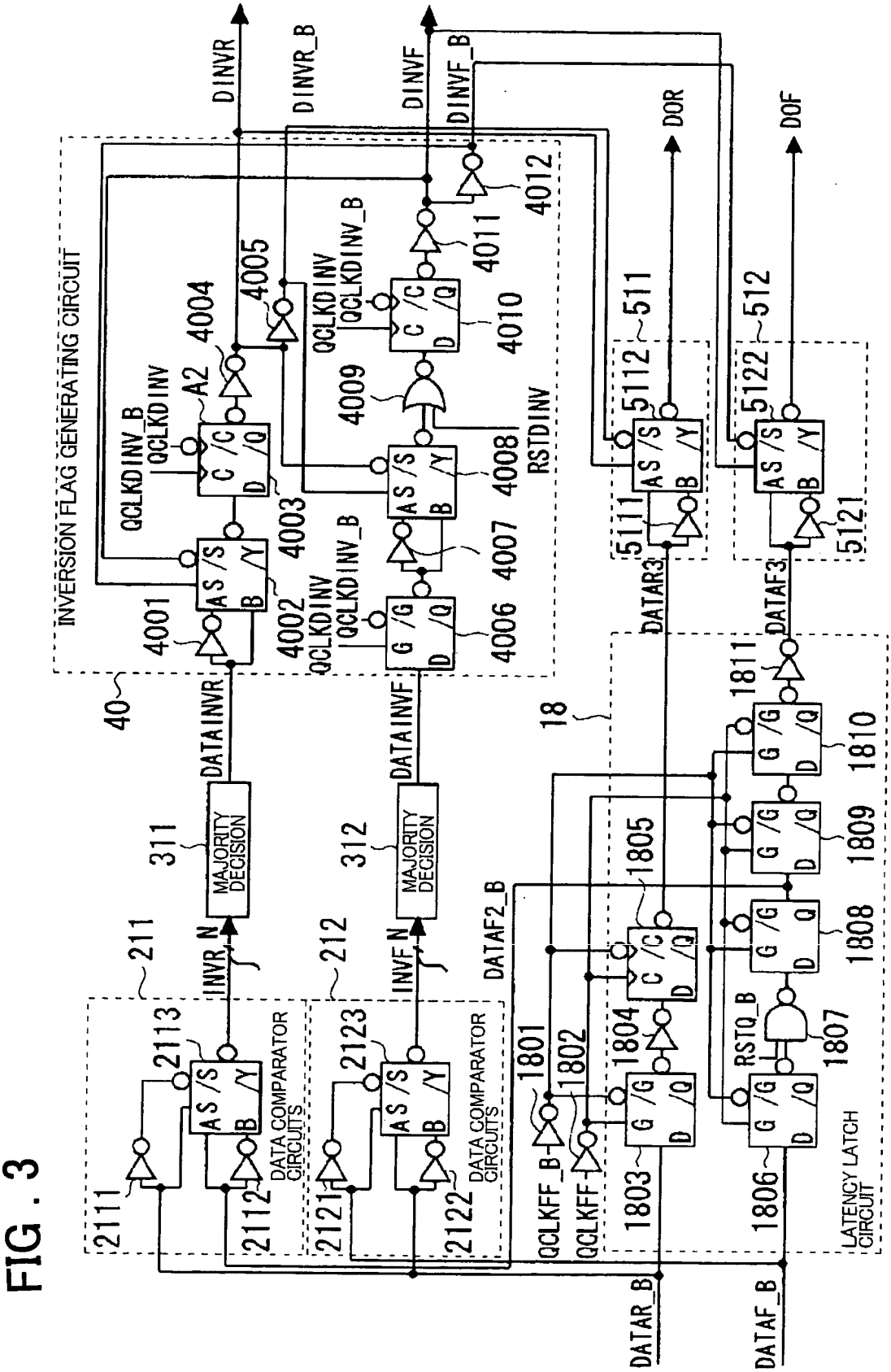

INVERSION FLAG GENERATING CIRCUIT
40
DINVR
DINVR_B
DINVF
DINVF_B
4001
4002
4003
4004
4005
4006
4007
4008
4009
4010
4011
4012
QCLKDINV
QCLKDINV_B
RSTDINV
DATAINVR
DATAINVF
311
312
MAJORITY DECISION
211
212
INVR_N
INVF_N
2111
2112
2113
2121
2122
2123
DATA COMPARATOR CIRCUITS
DATAF2_B
18
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
QCLKFF_B
QCLKFF
RSTQ_B
DATAR3
DATAF3
5111
5112
5121
5122
511
512
DOR
DOF
DATAR_B
DATAF_B
LATENCY LATCH CIRCUIT

FIG . 4A

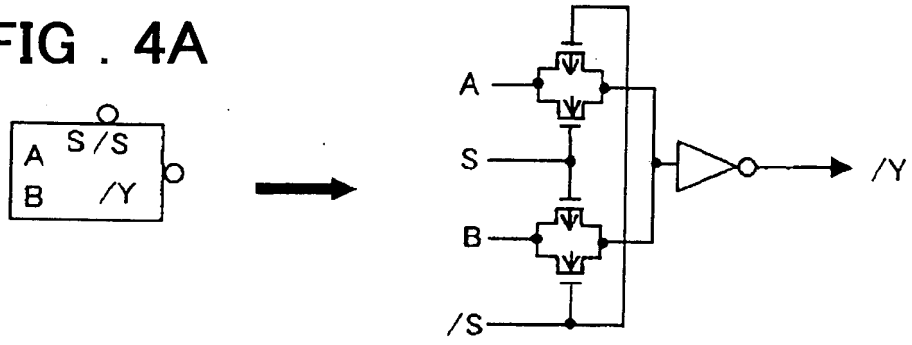


FIG . 4B

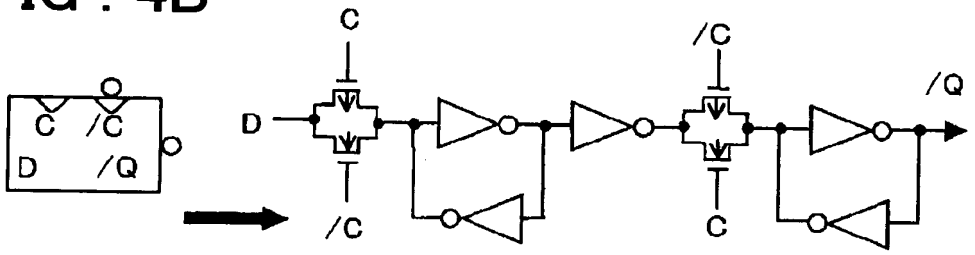


FIG . 4C

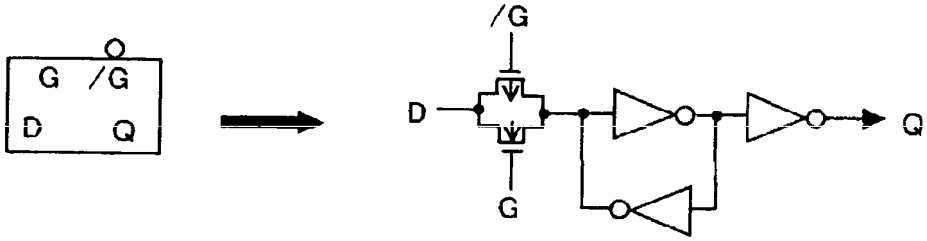


FIG . 4D

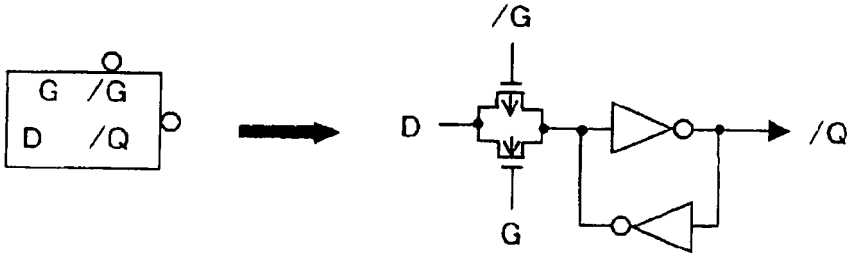


FIG . 5

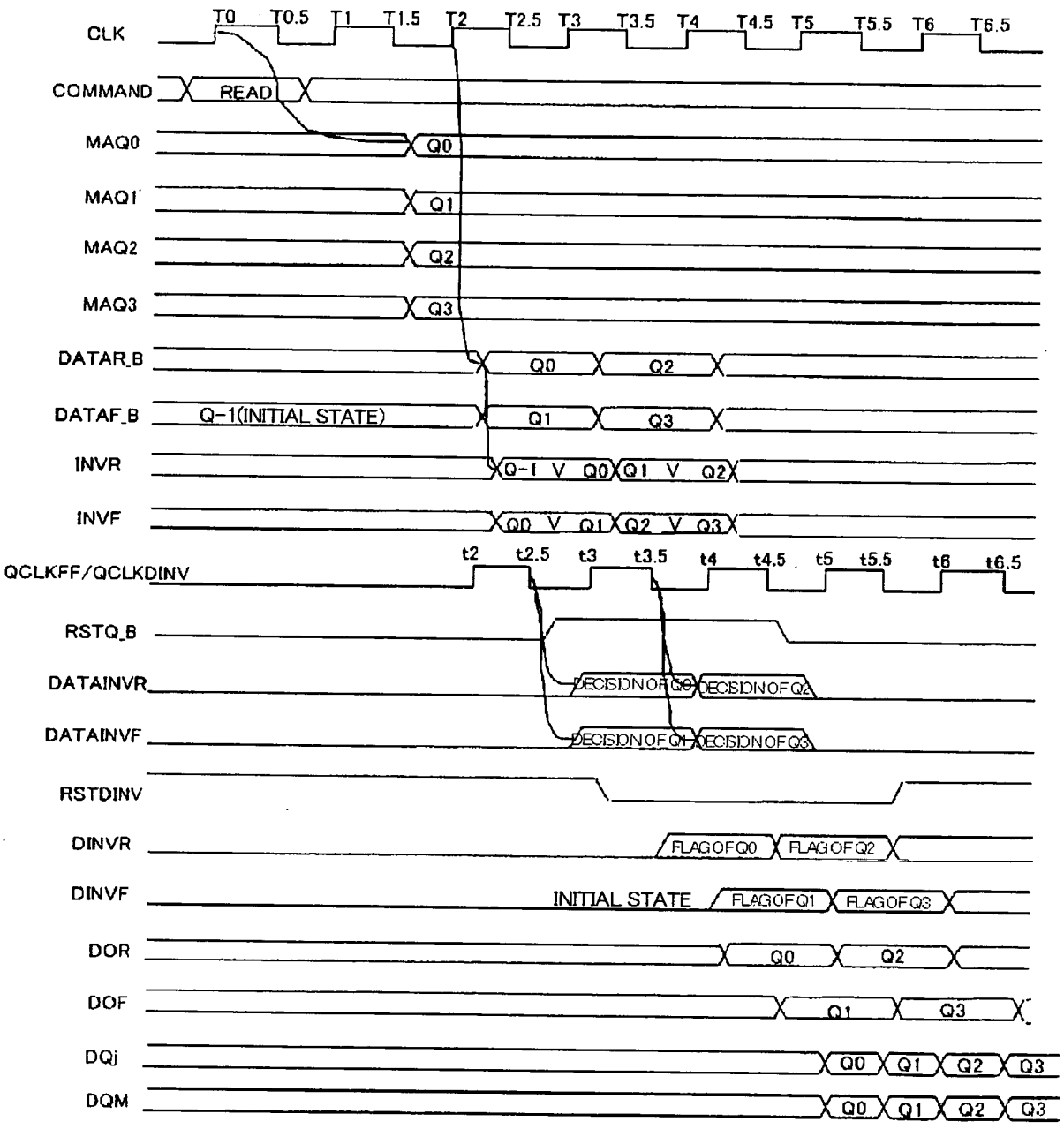
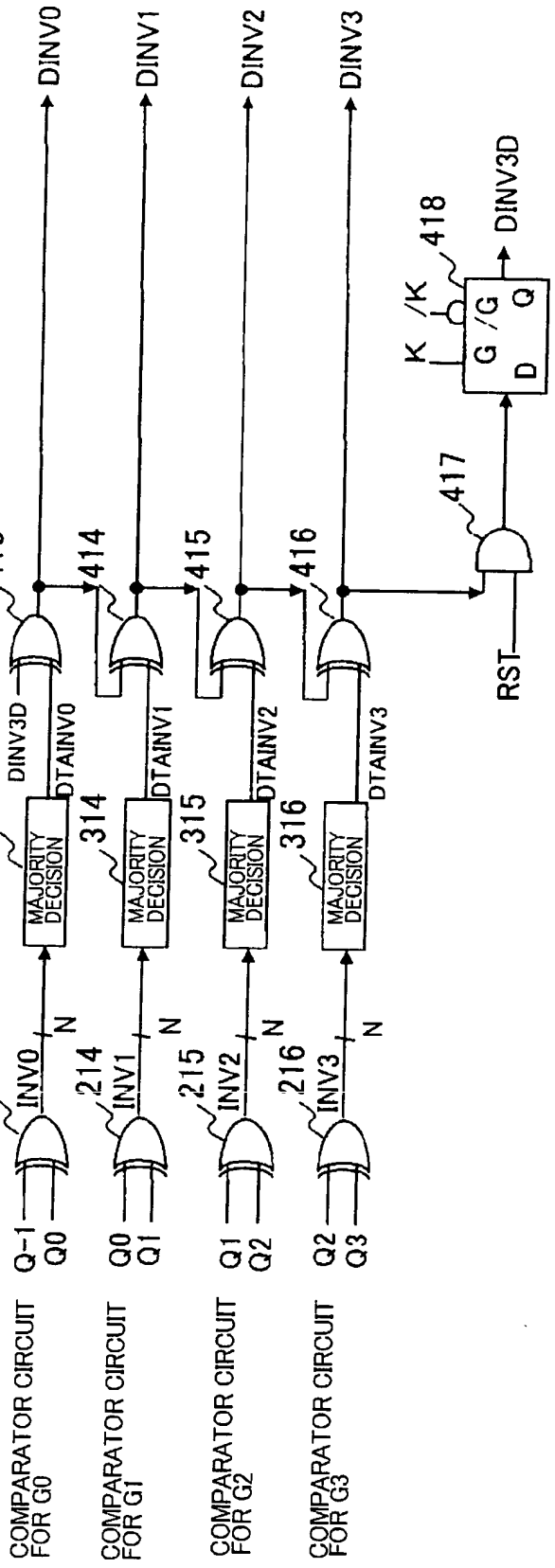

CLK
T0
T0.5
T1
T1.5
T2
T2.5
T3
T3.5
T4
T4.5
T5
T5.5
T6
T6.5
COMMAND
READ
MAQ0
Q0
MAQ1
Q1
MAQ2
Q2
MAQ3
Q3
DATAR_B
Q0
Q2
DATAF_B
Q-1(INITIAL STATE)
Q1
Q3
INVR
Q-1 V Q0
Q1 V Q2
INVF
Q0 V Q1
Q2 V Q3
QCLKFF/QCLKDINV
t2
t2.5
t3
t3.5
t4
t4.5
t5
t5.5
t6
t6.5
RSTQ_B
DATAINVR
DECISIONOFQ0
DECISIONOFQ2
DATAINVF
DECISIONOFQ1
DECISIONOFQ3
RSTDINV
DINVR
FLAGOFQ0
FLAGOFQ2
DINVF
INITIAL STATE
FLAGOFQ1
FLAGOFQ3
DOR
Q0
Q2
DOF
Q1
Q3
DQj
Q0
Q1
Q2
Q3
DQM
Q0
Q1
Q2
Q3

FIG . 6

CYCLE	DATAR	DATAF	INVR	INVF	DATAINVR	DATAINVF	DINVR	DINVF	DQj	DQM
INITIAL STATE		(0000000)						(Low)	(0000000)	
Q0,Q1	11111111	00000000	11111111	11111111	High	High	High	Low	00000000 00000000	High Low
Q2,Q3	11111111	00000000	11111111	11111111	High	High	High	Low	00000000 00000000	High Low

FIG. 7


COMPARATOR CIRCUIT FOR G0
COMPARATOR CIRCUIT FOR G1
COMPARATOR CIRCUIT FOR G2
COMPARATOR CIRCUIT FOR G3
Q-1
Q0
Q1
Q2
Q3
213
214
215
216
INV0
INV1
INV2
INV3
N
313
314
315
316
MAJORITY DECISION
DINV3D
DTAINV0
DTAINV1
DTAINV2
DTAINV3
413
414
415
416
DINV0
DINV1
DINV2
DINV3
417
RST
418
K
/K
G
/G
D
Q
DINV3D

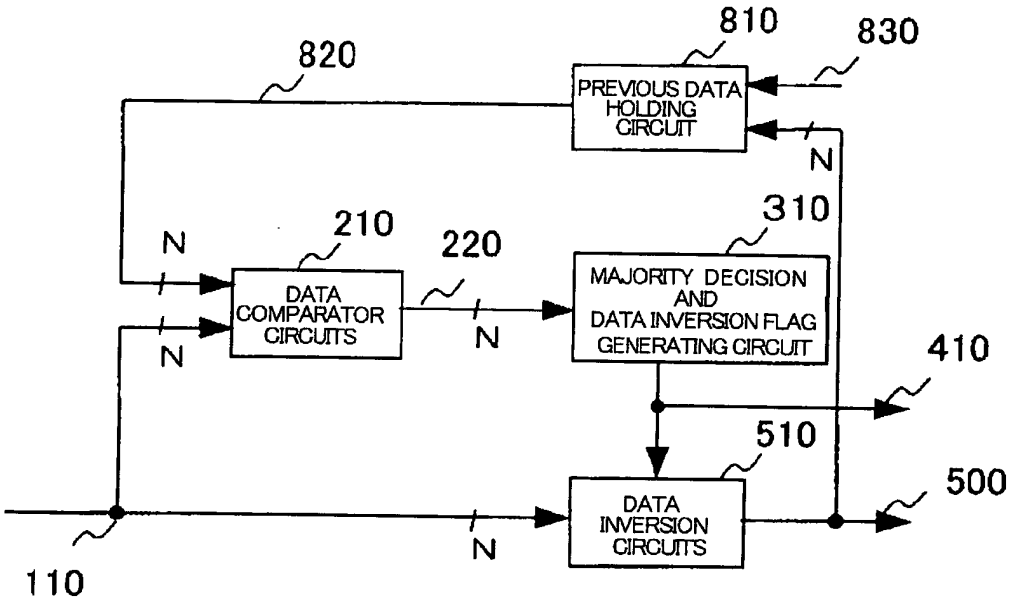



FIG . 8 PRIOR ART